

Electronic Acknowledgement Receipt

EFS ID:	2847487
Application Number:	10787488
International Application Number:	
Confirmation Number:	4982
Title of Invention:	INTEGRATED CIRCUIT LOGIC WITH SELF COMPENSATING BLOCK DELAYS
First Named Inventor/Applicant Name:	Puneet Gupta
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Attorney Docket Number:	YOR920040091US1
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	US_IDS_Form__SB_08a.pdf	779966 7118dcee882e590727c7b46cd6081a4132407487	no	4

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2	NPL Documents	YOR920040091-1.pdf	477200	no	8
			cd561d6d36e90b85144fb77b2fe36cd24ee3b29		

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3	NPL Documents	YOR920040091-2.pdf	873807	no	14
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4	NPL Documents	YOR920040091-3.pdf	810731	no	13
			86e6e650dcabdfbf172e2c9e81f535c235b5b71		

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5	NPL Documents	YOR920040091-4.pdf	193308	no	9
			03281a87238e4b9741a2d0f246b72665e59ab062		

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